

METHOD FOR FORMING A METALLIZATION LAYER

This application is a Divisional of U.S. Application No. 10/217,620, filed August 13, 2002, which is a Divisional of U.S. Application No. 09/652,619, filed
5 August 31, 2000, which is a Continuation of U.S. Application No. 08/912,051, filed August 18, 1997, now U.S. Patent No. 6,144,095, which is a Continuation of U.S. Application No. 08/656,712, filed June 3, 1996, now U.S. Patent No. 5,662,788.

Technical Field of the Invention

10 The present invention relates generally to integrated circuits and, in particular, to a method for forming a metallization layer.

Background of the Invention

An integrated circuit comprises a large number of semiconductor devices, such
15 as transistors, that are formed on a semiconductor substrate or, more colloquially, a "chip." These devices are selectively interconnected by one or more patterned layers of a conductive material, typically aluminum, to form a circuit that performs a desired function. These layers are referred to as "metallization" layers. As integrated circuits become more complex, designers reduce the minimum feature size of the constituent
20 devices of the circuit, so as to fit more devices on a chip. With this reduction in size, it becomes more difficult to achieve proper pattern definition using conventional techniques such as photolithography and dry etch techniques for forming metallization layers. Further, designers have attempted to use copper instead of aluminum as the principle metallization material in the metal-lization layers, due to perceived advantages
25 in resistivity, ductility and melting point. Unfortunately, developers have not been able to create a reliable technique for patterning a copper layer.

For example, one process using electro-deposition for forming a copper metallization layer is described in U.S. Patent No. 5,151,168. According to this process, a conductive barrier layer is deposited on a semiconductor substrate. Further, a

photoresist reverse image of the maskwork normally used to etch the metallization pattern is created on the substrate. The wafer is then transferred to an electrolytic bath in which the copper is complexed with EDTA molecules. A fixed voltage is applied between a voltage source and the semiconductor substrate to deposit the copper ions on
5 the barrier layer that is not covered by the photoresist layer including contact/via openings on the semiconductor substrate. Unfortunately, when the substrate is placed in the electrolytic bath, the photoresist material may lift-off from the substrate thus depositing copper in areas where it is not required.

For the reasons stated above, and for other reasons stated below which will
10 become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a method for forming a metallization layer that avoids the disadvantages and problems of prior techniques.

Summary of the Invention

15 A method for forming a metallization layer is described which uses a single electro-deposition step to reliably form both the metallization layer and to fill the contact vias. In particular, one embodiment of the present invention uses first and second layers of materials that are placed at different surface potentials to form the metallization layer. The first layer is formed outwardly from a semiconductor substrate.
20 Contact vias are formed through the first layer to the semiconductor substrate. The second layer is formed outwardly from the first layer. Portions of the second layer are selectively removed such that the remaining portion of the second layer defines the layout of the metallization layer and the contact vias. Metal ions in a solution are electro-deposited by applying a bi-polar modulated voltage having a positive duty cycle
25 and a negative duty cycle to the layers and the solution. The voltage and surface potentials are selected such that the metal ions are deposited on the remaining portions of the second layer. Further, metal ions deposited on the first layer during a positive duty cycle are removed from the first layer during a negative duty cycle. Finally, exposed portions of the first layer are selectively removed.

In another embodiment of the present invention, the first and second layers are placed at different surface potentials by applying a first voltage to a surface of the first layer and applying a second voltage, higher than the first voltage, to the second layer. In another embodiment of the present invention the different surface potentials are
5 achieved in part by selecting materials for the first and second layers that have different innate surface potentials.

Brief Description of the Drawings

Figures 1A through 1D are cross-sectional views of a semiconductor substrate
10 that illustrate process steps according to an illustrative embodiment of the present invention.

Figures 2 and 3 are cross-sectional views of additional illustrative embodiments of the present invention.

Detailed Description of the Invention

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These
15 embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be used and that logical, mechanical and electrical changes may be made without departing from the spirit and scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense.

Figures 1A through 1D are cross-sectional views of semiconductor substrate 10
25 that depict process steps according to an illustrative embodiment of the present invention. Advantageously, the illustrative embodiment forms a metallization layer, including filling contact vias, outwardly from semiconductor substrate 10 in a single electro-deposition step. The process exposes adjacent layers of materials that are formed outwardly from semiconductor substrate 10 with different surface potentials to a

bi-polar modulated voltage source to deposit the metallization layer and to fill the contact vias. The surface potentials and the modulated voltage are selected such that the metallization layer forms only on the second layer because metal that deposits on the first layer during a first duty cycle of the bi-polar modulated voltage is removed from
5 the first layer during a second duty cycle.

As shown in Figure 1A, borophosphosilicate glass (BPSG) layer 12 is deposited and reflowed outwardly from semiconductor substrate 10. First layer 14 is formed outwardly from BPSG layer 12. First layer 14 may comprise, for example, poly-silicon, doped or undoped, that is deposited using a conventional chemical vapor deposition
10 (CVD) or sputtering technique. Alternatively, other materials such as germanium may be substituted for the poly-silicon. Contact via 16 is etched through first layer 14 and BPSG layer 12 to, for example, junction 18 of semiconductor substrate 10. Second layer 20 is formed outwardly from first layer 14 so as to line contact via 16 and cover first layer 14 by, for example, depositing a layer of titanium nitride or other appropriate
15 barrier layer material using a conventional sputter or chemical vapor deposition technique. First layer 14 and second layer 20 have a thickness on the order of 100 to 500 Å. Advantageously, the innate surface potential of first layer 14 is lower than the innate surface potential of second layer 20. This difference in surface potentials contributes to the selectivity of the electro-deposition step described below. In other
20 embodiments, first and second layers 14 and 20 can be fabricated from other materials that provide similar differences in innate surface potential.

Portions of second layer 20 are selectively removed such that the remaining portions of second layer 20 match the desired pattern for the metallization layer, including contact vias. As shown in Figure 1B, layer 22, comprising, for example, a
25 conventional photoresist material, is formed outwardly from layer 20 using conventional techniques. Layer 22 is exposed through a mask. Portions of layer 22 are removed with a solvent so as to produce a patterned layer of photoresist material that matches the desired metallization layer. The exposed portions of layer 20 are removed with, for example, a dry etch leaving a patterned version of layer 20. Layer 22 is removed.

Once layer 20 is patterned, semiconductor substrate 10 is placed in an electrolytic bath for electro-deposition of the metallization layer outwardly from layer 20 so as to fill contact vias 16. The bath includes metal ions in a solution. For example, the metal ions may comprise copper ions in a solution as described in U.S. Patent No. 5,151,168 entitled "Process for Metallizing Integrated Circuits With Electrically-Deposited Copper" (the "'168 Patent"), the teachings of which are incorporated by reference. Specifically, one embodiment of the electrolytic bath is described in the '168 Patent at Column 5, lines 10 through 35. Alternatively, the electrolytic bath may comprise a solution containing nickel or palladium ions.

10 Voltage source 26 provides a bipolar modulated voltage to anode 28 and voltage source 24 provides a DC offset voltage to anode 28. The voltage on anode 28 causes metal ions to be deposited on a layer when the potential difference between anode 28 and the surface potential of the layer exceeds the reduction potential of the metal. Conversely, the voltage on anode 28 causes metal ions to be removed from the surface
15 of a layer when the potential difference between anode 28 and the surface potential of the layer is less than the reverse deposition potential of the metal. The voltages of sources 26 and 28 are selected such that metal deposited on layer 14 during a first duty cycle is removed during a second duty cycle. Further, metal is not removed from layer 20 during the second duty cycle. For example, in one embodiment source 26 provides a
20 square wave with a dc offset provided by source 24 such that during the positive duty cycle of source 26, metal ions deposit on layers 14 and 20 and during the negative duty cycle copper is etched from layer 14. In other embodiments, source 26 comprises other time-varying wave-forms such as a triangle wave, sinusoidal wave or other appropriate voltage wave form.

25 Once the deposition of metallization layer 30 is complete, exposed portions of first layer 14 are removed leaving the structure shown in Figure 1D. In one embodiment, metallization layer 30 covers all of the exposed surfaces of layer 20 as shown in Figure 2. It is understood that an integrated circuit constructed according to this process would include a complete metallization layer with a plurality of contact vias

even though only portions of the metallization layer and a single contact via are shown in Figures 1A through 1D.

Conclusion

5 Although an illustrative embodiment has been described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the illustrative embodiment. For example, the type of modulated voltage can be varied from the
10 specified square wave used in the illustrative embodiment. Further, the difference in surface potential between layers 14 and 20 can be imposed or enhanced by applying voltages to the surfaces of layers 14 and 20. In this embodiment, layers 14 and 20 are separated by insulating layer 15 as shown in Figure 3. The composition of the electrolytic bath can be varied so long as metal ions deposit on layer 20 when sources 24
15 and 26 are applied to anode 28.